AND8443/D

Timing-Safe™ Spread Spectrum EMI Reduction

ON Semiconductor®

www.onsemi.com

APPLICATION NOTE

Conventional Spread Spectrum

Spread spectrum electromagnetic interference (EMI) reduction is a technique in which the frequency of a clock signal is increased or decreased gradually, and then brought back to its original frequency. By "spreading" electromagnetic energy over a narrow band of the frequency spectrum, the energy spikes of the frequencies and harmonics are smoothed over, hence reducing EMI. The technique is effective when applied to systems where a single master clock acts as the source of the system timing and all other clock and data signals derive their timing from this source. However, it can invite data synchronization problems when attempts are made to use this technique directly on selected independent sub-system clocks.

What is Timing-Safe™?

Timing-Safe technology solves a major drawback of traditional spread spectrum EMI reduction—the potential misalignment of clock and data paths. Timing-Safe achieves this by limiting variations in signal frequencies to defined regions corresponding to clock edges. The technique effectively reduces the peak amplitudes of clock signals—thereby ensuring compliance with FCC standards—while maintaining synchronization throughout the system and protecting data integrity.

Faster data rates have made EMI FCC compliance a difficult challenge. The designer's first choice is to spread the master clock at its origin. This approach keeps the data and the clock synchronized throughout the system. Often the master clock gets distributed to multiple sub-systems. Several sub-systems could function well with the master clock having spread spectrum. In certain designs; however, sub-system clocks may require independent EMI spreading. In such a case, the data and the clock can lose synchronization, manifesting itself as cycle slip. A Timing-Safe buffer provides spread spectrum clock modulation for EMI reduction without the associated cycle slip. These devices can be inserted directly into the sub-system clock path as an Active Bead™ EMI filter. This allows a true drop-in solution to reduce sub-system EMI.

Typical SDRAM System without Spread Spectrum Clock

A typical SDRAM platform is illustrated in the example below (Figure 1). In this configuration, EMI is often found to be radiating from the SDRAM clocks.

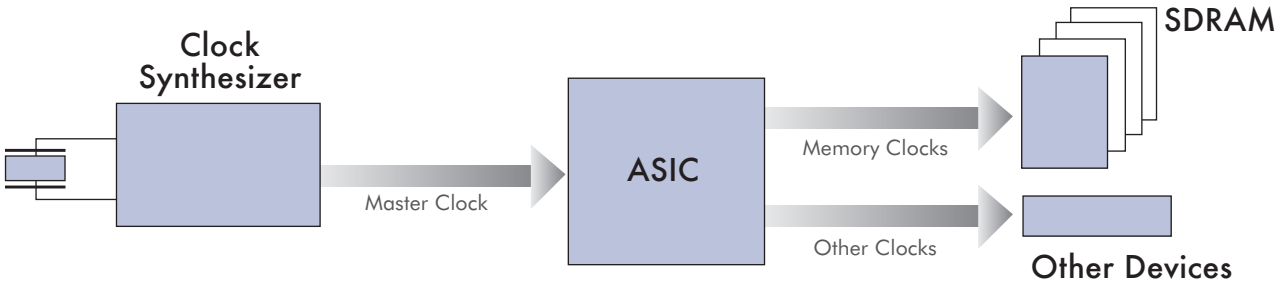

Figure 1.

Typical SDRAM System with Spread Spectrum Clock

If the typical SDRAM platform requires EMI reduction, the standard practice is to apply spread spectrum at the source clock synthesizer, shown below (Figure 2). When using standard spread spectrum clocking (SSC) the only viable placement is at the source (system) clock.

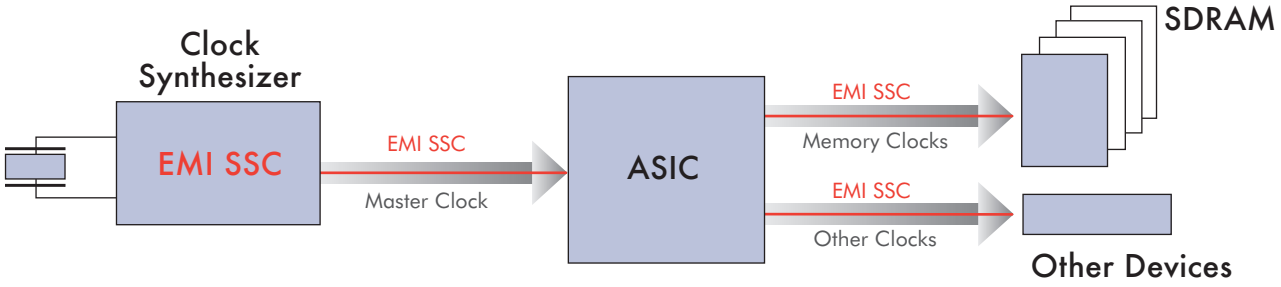

Figure 2.

There are possible issues when placing the standard SSC at the source to an application-specific integrated circuit (ASIC). For example, if the ASIC integrates a TV encoder then the standard SSC cannot be used at the source (to lower SDRAM EMI), as the TV encoder cannot function correctly with SSC. Nor can the conventional SSC integrated circuit (IC) be placed directly on the SDRAM clock trace as this will cause cycle slippage and phase shift between the clock and data signals.

SDRAM System with Timing-Safe EMI Reduction

The Timing-Safe clock buffer allows Spread Spectrum EMI reduction to be inserted directly onto the SDRAM memory clock distribution lines (Figure 3). This solution is independent of the ASIC, and does not affect other areas of the system.

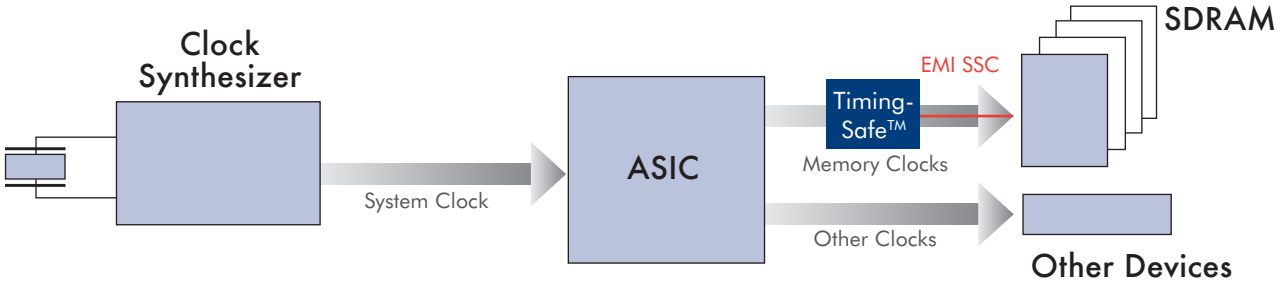

Figure 3.

Timing-Safe/SSC Difference

The waveform difference between Timing-Safe and regular SSC is shown below. Note that using a Timing-Safe clock, the spread spectrum signal is confined to a defined region, guaranteeing that the clock signal never loses synchronization with the data. The clock can be seen clearly (Figure 4). On the other hand, a standard SSC clock is spread without regard to data timing (Figure 5). The clock is grossly misaligned and is no longer synchronous (Figure 5).

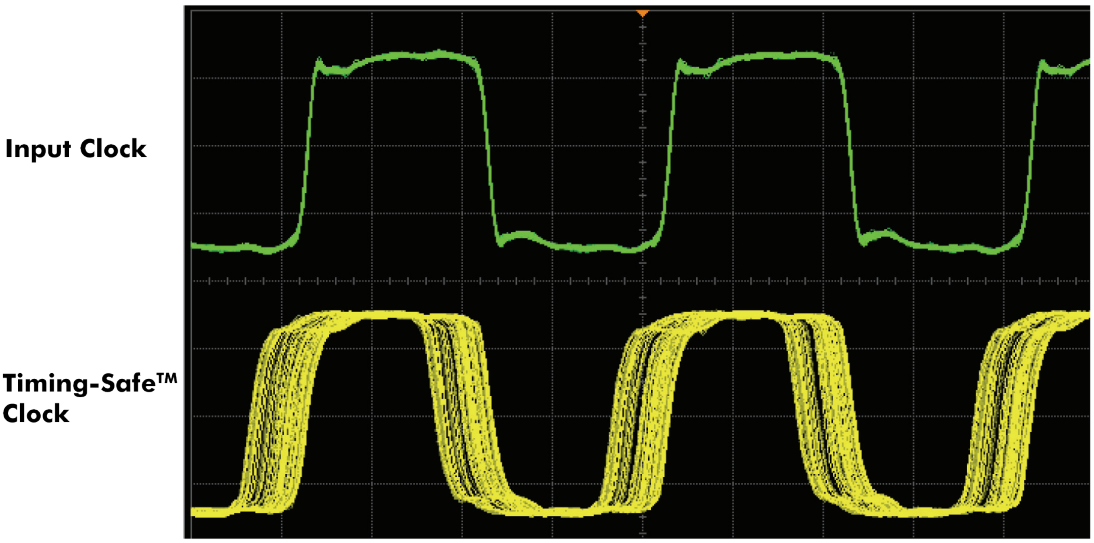

Figure 4. Timing-Safe Clock

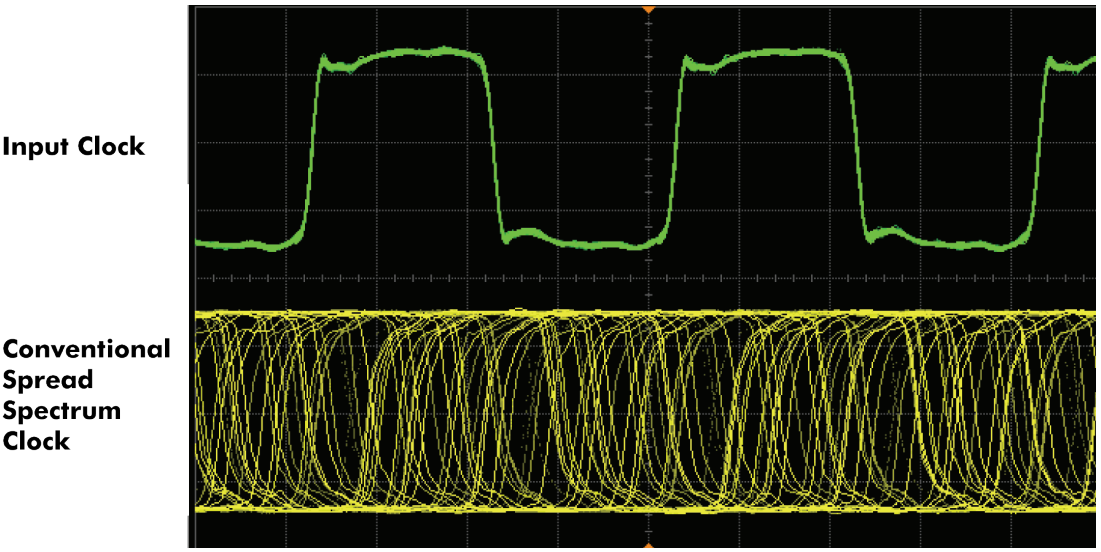

Figure 5. SSC Clock

Figure 6 shows the spectral response of a Timing-Safe buffer with Spread Spectrum turned off. When Timing-Safe Spread Spectrum is enabled, as shown in Figure 7, the amplitude of the spectral harmonics is reduced significantly. This reduction is achieved while maintaining constant data synchronization.

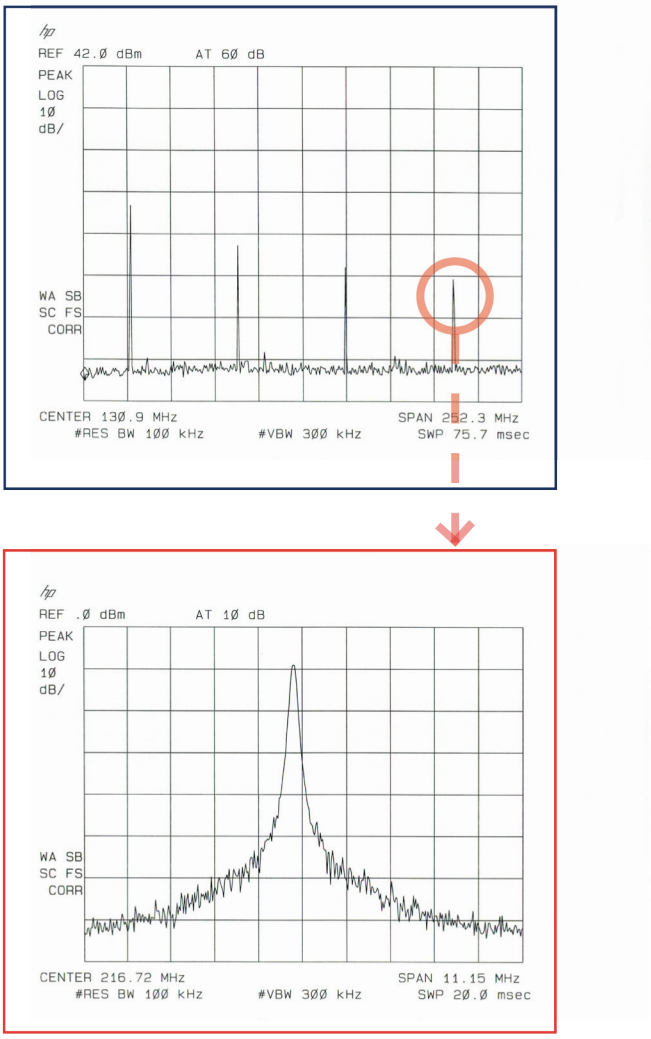

Figure 6. Before Timing-Safe.

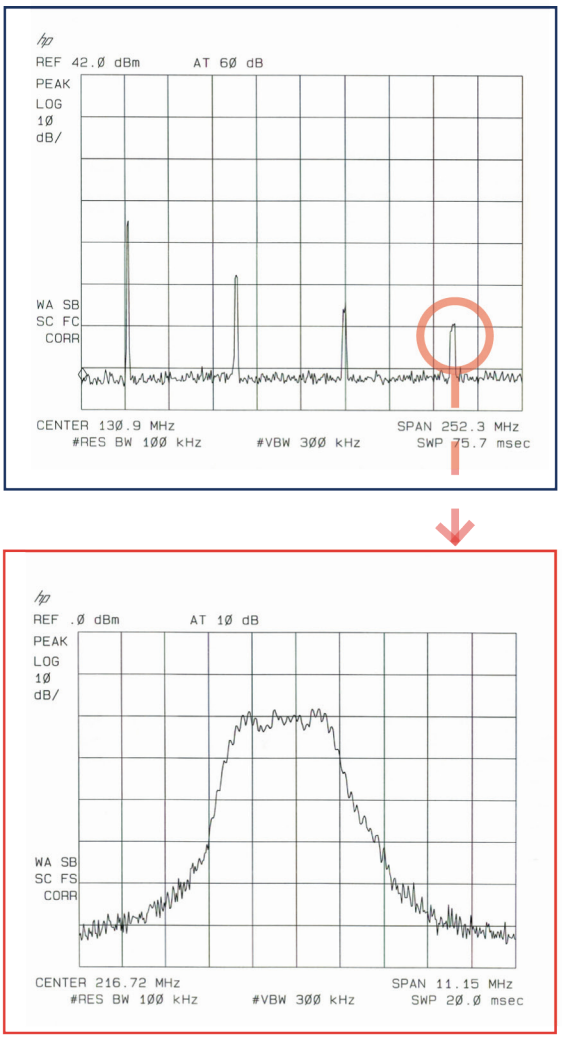

Figure 7. After Timing-Safe.

Conclusion

Timing-Safe EMI reduction Spread Spectrum is ideal in high-speed clock platforms, including SDRAM systems. It provides all the benefits of spread spectrum with the added benefit of data integrity, allowing system designers the added flexibility to target specific areas for EMI reduction and FCC compliance platforms.

For more information visit **www.onsemi.com**.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada.
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative